IN THE CLAIMS:

Claim 1 (currently amended): A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

a redistribution layer having a plurality of electrode pads and electrical conductive patterns connecting the electrodes of the semiconductor element to the respective electrode pads;

a plurality of metal posts each with a first shape and a first size formed on the electrode pads of the redistribution layer, the metal posts being configured to be provided with external connection electrodes; and

at least one mark member with a second shape and a second size which serves as an alignment mark located in a predetermined positional relationship with the metal posts,

wherein the mark member is made of the same material as the metal posts; and

wherein the first shape and the first size are correspondingly different from the second shape and the second size.

Claim 2 (previously presented): The semiconductor device as claimed in claim 1, wherein the alignment mark has an outer configuration other than a circle.

Claim 3 (previously presented): The semiconductor device as claimed in claim 1, wherein a width of the alignment mark measured along a plane parallel to a surface of the redistribution layer is greater than a height of the metal posts.

Claim 4 (currently amended): A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

a redistribution layer having a plurality of conductive patterns which connects the electrodes of the semiconductor device to a plurality of electrode pads each with a first shape and a first size located in predetermined positions of the redistribution layer; and

at least one mark member with a second shape and a second size which serves as an alignment mark located in a predetermined positional relationship with the electrode pads;

wherein the mark member is made of the same material ~~with~~ as the electrode pads; and

wherein the first shape and the first size are correspondingly different from the second shape and the second size.

Claim 5 (previously presented): The semiconductor device as claimed in claim 4, wherein the alignment mark has an outer configuration other than a circle.

Claim 6 (original): A method of testing a semiconductor device, comprising the steps of:

forming a redistribution layer on the semiconductor device in a wafer state;

forming metal posts on the redistribution layer;

forming a mark member in a predetermined position on the redistribution layer with respect to the metal posts, the mark member serving as an alignment mark; and

performing a semiconductor test while determining positions of electrodes of the semiconductor device by recognizing the alignment mark.

Claim 7 (original): The method as claimed in claim 6, wherein the step of forming a mark member includes the step of forming at least two mark members on the redistribution layer in a periphery of the wafer.

Claim 8 (original): A method of testing a semiconductor device, comprising the steps of:

forming a redistribution layer on the semiconductor device in a wafer state; and

encapsulating the wafer with a seal resin while maintaining a periphery of the wafer unsealed, the periphery of the wafer corresponding to an area other than an area in which the semiconductor device is formed.

Claim 9 (original): The method as claimed in claim 8, further comprising th step of forming an alignment mark on the periphery of the wafer, the alignment mark being used for recognition of a position of the semiconductor device.

Claim 10 (original): A method of testing semiconductor devices, comprising the steps of:

forming a redistribution layer on the semiconductor devices in a wafer state;

forming a seal resin layer on the redistribution layer so as to encapsulate the semiconductor devices;

forming grooves in the seal resin layer along scribe lines, the grooves extending through the seal resin layer so that a bottom of each of the grooves reaches the wafer;

performing a test on the semiconductor devices in the wafer state while recognizing the wafer exposed on the bottom of the groove as a reference position; and

separating the wafer into individual semiconductor devices by cutting the wafer along the scribe lines.

Claim 11 (original): The method as claimed in claim 10, wherein the step of forming grooves includes the step of forming grooves along predetermined scribe lines selected from all of the scribe lines provided for the wafer.

Claim 12 (original): A method of fixing a wafer onto a vacuum chuck table by suction, comprising the steps of:

suctioning a portion of the wafer having a minimum warp so that the portion of the wafer is fixed onto the vacuum chuck table;

suctioning a portion of the wafer adjacent to the suctioned portion of the wafer so that the portion of the wafer adjacent to the suctioned portion is fixed onto the vacuum chuck table; and

sequentially repeating the suctioning step until an entire wafer is fixed onto the vacuum chuck table by suction.

Claim 13 (currently amended): An apparatus for fixing a semiconductor wafer by suction, comprising:

a vacuum chuck table having a porous plate overlaying a plurality of concentric suction grooves;

a plurality of suction passages each being correspondingly connected to the plurality of concentric suction grooves ~~each barometrically independent from another~~; and

each of the plurality of suction passages being connected to more than one hole on the porous plate;

suctioning device for sequentially introducing a suctioning force into the suction passages at different timing.

Claim 14 (currently amended): A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

a redistribution layer having a plurality of electrode pads and electrical conductive patterns connecting the electrodes of the semiconductor element to the respective electrode pads;

a plurality of metal posts with a first shape and a first size formed on the electrode pads of the redistribution layer, the metal posts being configured to be provided with external connection electrodes; and

at least one mark member with a second shape and a second size which serves as an alignment mark located in a predetermined positional relationship with the metal posts;

wherein the first shape and the first size are correspondingly different from the second shape and the second size.

Claim 15 (currently amended): A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

a redistribution layer having a plurality of electrode pads and electrical conductive patterns connecting the electrodes of the semiconductor element to the respective electrode pads;

a plurality of metal posts formed on the electrode pads of the redistribution layer;

at least one electrode part comprising one of the metal posts and a protruding electrode attached to a top of the one of the metal posts; and

at least one mark member which serves as an alignment mark located in a predetermined positional relationship with the electrode part, the mark member comprising one of the metal posts but lacking the protruding electrode.